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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 4

Complete if Known	
Application Number	10/648,434
Filing Date	August 27, 2003
First Named Inventor	Sanjay DABRAL
Group Art Unit	2822
Examiner Name	Not Yet Assigned
Attorney Docket Number	2207/597504

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number – Number – Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JZ		US- 5,461,338	10-24-95	Hirayama et al.	
JZ		US- 5,557,231	09-17-96	Yamaguchi et al.	
JZ		US- 5,559,368	09-24-96	Hu et al.	
JZ		US- 5,689,144	11-18-97	Williams	
JZ		US- 5,689,209	11-18-97	Williams et al.	
JZ		US- 6,493,430	12-10-02	Leuca et al.	
JZ		US- 6,100,751	08-08-00	De et al.	
JZ		US- 6,218,895	04-17-01	De et al.	
JZ		US- 6,300,819	10-09-01	De et al.	
JZ		US- 6,166,584	12-26-00	De et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document – Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
JZ		WO 98/59419	16 JUNE 1998	DE et al.		

Examiner Signature	Jeffrey Zweizig	Date Considered	5/25/04

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First Named Inventor	Sanjay DABRAL et al.
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
JZ		Excerpt from "1996 IEEE International SOI Conference Proceedings" (October 1996) p. 141.	
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JZ		ASSADERAGHI, F. et al., "High-Performance Sub-Quarter-Micrometer PMOSFET's on SOI", *IEEE Electron Device Letters*, Vol. 14, No. 6 (June 1993) pp. 298-300.	
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Examiner Signature	Jeffrey Zweizig	Dat Considered	5/25/04

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JZ		KURODA, T. et al., "A 0.9-V, 150-MHz, 10-mW, 4mm^2, 2-D Discrete Cosine Transform Core Processor With Variable Threshold-Voltage (VT) Scheme", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 11 (November 1996) pp. 1770-1779.	
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JZ		WALKER, W. et al., "Design And Analysis Of A CMOS SOS/SOI Receiver For A Radiation Hard Computer", *IEEE SOS/SOI Technology* Conference, (October 1989) pp. 167-168.	
JZ		WANN, H. Clement et al., "Channel Doping Engineering Of MOSFET With Adaptable Threshold Voltage Using Body Effect For Low Voltage And Low Power Applications", *International Symposium On VLSI Technology, Systems and Applications - Proceedings Of Technical Papers*, (1995) pp. 159-163..	
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